I CLAIM:

1. A high capacity packet switch, comprising:

a plurality of core modules, each of the core modules operating in a circuit switching mode;

a plurality of edge modules connected to subtending packet sources and subtending packet sinks, each of the edge modules operating in a packet switching mode;

wherein the core modules switch payload traffic between the edge modules using wavelength division multiplexing (WDM) and time division multiplexing (TDM).

2. A high capacity packet switch as claimed in claim 1 wherein each core module is a space switch.

3. A high capacity packet switch as claimed in claim 2 wherein each core module is a single-stage electronic rotator switch.

4. A high capacity packet switch as claimed in claim 1 wherein:

each edge module has a plurality of ingress ports, each of the ingress ports having an associated ingress queue; and

an ingress scheduler sorts packets arriving in the ingress queues from the subtending packet sources, the sort being by egress edge module from which the respective packets are to egress from the high capacity packet switch for delivery to the subtending packet sinks.

5. A high capacity packet switch as claimed in claim 4 wherein the ingress scheduler periodically determines a number of packets waiting in the ingress queues for each respective egress edge module and sends a capacity request vector to each of the controllers of the core modules, the capacity request vector sent to a given controller relating only to a group of channels that connect the edge module to the given core module.

6. A high capacity packet switch as claimed in claim 5 wherein each ingress edge module maintains a vector of pointers to the packets sorted by egress edge module and a scheduling matrix that provides a port number for each slot in which a data block can be transferred, the scheduling matrix being arranged in the same egress edge module order so that the scheduling matrix and the pointers are logically aligned; and, when a non-blank entry in the scheduling matrix indicates an egress port through which a data block can be transferred, a corresponding pointer in the vector of pointers is used to locate a starting point for the data block in the packets waiting in the ingress queues.

7. A high capacity packet switch as claimed in claim 1 wherein the core modules and the edge modules are spatially distributed.

8. A high capacity packet switch as claimed in claim 7 wherein one edge module is co-located with each core module, and the edge module serves as a controller for the core module.

9. A high capacity packet switch as claimed in claim 8 wherein each edge module has *M* reconfiguration timing circuits, where *M* is the number of core modules, each of the reconfiguration timing circuits being time-coordinated with a time counter in the respective edge modules that serve as processors for the core modules, to coordinate data transfer from the ingress edge modules when the core modules are reconfigured to change channel connectivity.

10. A high capacity packet switch as claimed in claim 1 wherein each edge module is connected to each core module by at least one communications link.

11. A high capacity packet switch as claimed in claim 10 wherein each core module comprises a plurality of single-stage rotator switches, each rotator switch having a number of input ports collectively adapted to accommodate a number of channels equal to the number of ingress edge modules and a number of output ports collectively adapted to accommodate a number of channels equal to the number of egress edge modules, and each edge module has at least one channel to each of the rotator switches.

12. A high capacity distributed packet switch, comprising:

a plurality of distributed core modules, each core module having a plurality of input ports and a plurality of output ports, the distributed core modules switching payload traffic in a circuit switching mode; and

a plurality of distributed ingress edge modules, each ingress edge module having a plurality of ingress ports for receiving payload traffic from subtending sources and a plurality of egress ports for transferring payload traffic to the core modules;

a plurality of egress edge modules having a plurality of ingress ports for receiving payload traffic from the core modules and a plurality of egress ports for transferring the payload traffic to subtending sinks; and

each of the ingress and egress edge modules operates in a packet switching mode.

13. A high capacity distributed packet switch as claimed in claim 12 wherein the ingress edge modules and the egress edge modules comprise integrated units of one ingress edge module and one egress edge module each.

14. A method of switching payload data packets through a distributed data packet switch, comprising the steps of:

a) receiving a payload data packet from a subtending source at an ingress edge module of the distributed data packets switch;

b) determining an identity of an egress edge module from which the data packet should egress from the distributed data packet switch;

c) arranging the data packet in a sorted order with other data packets received so that the data packets are arranged in a sorted order corresponding to the identity of the edge module from which the data packet should egress from the distributed data packet switch;

d) transferring the sorted data packets in fixed-length data blocks to a core module of the distributed data packet switch;

e) switching the fixed-length data blocks through the core module to the egress module; and

f) transferring the payload data packet from the egress module to a subtending sink.

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